We claim:

1. A method for making a semiconductor structure in a substrate having an array area and a periphery area, the method comprising:

forming a transistor in the array area and a transistor in the periphery area;

forming a stopping layer over the transistors in the array area and the periphery area, the stopping layer having a characteristic to stop an etching process when consumed by the etching process;

forming over the stopping layer a nonconductive layer;

forming openings by etching the nonconductive layer and the stopping layer; and

forming a metallization layer by filling the openings with conductive substances and compounds, the metallization layer forming a local interconnect layer for the transistor in the array area and forming a strapping layer for the transistor in the periphery area.

2. The method of claim 1, wherein forming openings includes forming openings by a self-aligned contact (SAC) etching technique.

3. The method of claim 1, wherein forming openings includes forming openings on gate structures in the high-density area to form contacts and forming openings on gate structures in the high-speed area so as to strap.

4. The method of claim 1, wherein forming a metallization layer includes forming a metallization layer that includes over-gate routings in the periphery area, slot holes in the periphery area, and contact holes in the periphery area.

5. The method of claim 1, wherein forming a metallization layer includes forming a silicide compound, forming a barrier layer, and forming a conductive layer.

6. A method for making a semiconductor structure in a semiconductor substrate having an array and a periphery, the method comprising:

depositing a nonconductive stack over a gate and source/drain of a memory cell in the array and over a gate of a transistor in the periphery, the nonconductive stack including a stopping layer and a nonconductive layer;

photolithographing to mark portions of the array and the periphery, the portions of the array including portions that are superjacent to the gate and source/drain of the memory cell in the array, the portions of the periphery includes portions that are superjacent to the gate of the transistor;

removing the portions of the array and the periphery that are marked to expose the gate and source/drain of the memory cell in the array and to expose the gate of the transistor in the periphery; and

depositing simultaneously local interconnect materials into portions of the array and the periphery that were removed by the act of removing.

7. The method of claim 6, wherein photolithographing includes photolithographing to mark portions of an array and a periphery, wherein a portion of the array includes local interconnect, and wherein a portion of the periphery includes gate straps, contact holes, contact slots, and local routing.

8. The method of claim 7, wherein removing includes etching away the revealed portions of the array so as to open up selected areas of the portion of the array and the portion of the periphery, wherein etching includes etching using a dry etch technique.

9. The method of claim 8, wherein depositing includes depositing simultaneously local interconnect materials, wherein the local interconnect materials include a combination of a substance to form a silicide, a barrier substance, and a substance to form a main conductive layer.

10. The method of claim 9, wherein depositing includes depositng simultaneously local interconnect materials, wherein the local interconnect materials includes titanium, titanium nitride, and tungsten.

11. A method for making a semiconductor structure in a substrate having an array and a periphery, comprising:

photolithographing to mask portions of gates in the array and the periphery;

dry-etching portions of the gates that are masked;

depositing over the gates a nonconductive stack having a stopping layer;

photolithographing portions of the array and the periphery that include the gates;

dry-etching the portions of the array and the periphery until stopped by the stopping layer; and

depositing simultaneously local interconnect materials into portions of the array and the periphery that are etched by the act of dry-etching.

12. The method of claim 11, further comprising depositing a group of materials to form gate structures, wherein the group of materials include a combination of a gate oxide material, polycrystalline silicon, a conductive material, and a cap dielectric material, wherein the conductive material include a conductor material and/or a barrier material, and wherein the act of depositing a group of materials to form gate structures occurs before the act of photolithographing to expose gate structures in an array and a periphery.

13. The method of claim 12, wherein photolithographing to mask portions of gates in an array and a periphery includes photolithographing to exhume contact in a portion of gate structures in the array and to open the portion of gate structures in the periphery so as to strap a conductive material to the portion of the gate structures in the periphery.

14. The method of claim 13, wherein dry-etching includes dry-etching a portion of the conductive material and the cap dielectric material.

15. The method of claim 14, further comprising stripping a resist that is formed by photolithographing, forming spacers, depositing a dielectric liner, and depositing borophosphosilicate glass.

16. The method of claim 15, wherein dry-etching the portions of the array and the periphery that are exposed includes etching to remove a portion of the borophosphosilicate glass and a portion of the dielectric liner.

17. The method of claim 16, further comprising depositing a substance to form a silicide compound, a barrier compound, and a conductive substance.

18. The method of claim 17, further comprising planarizing using a chemical-mechanical planarization technique to planarize the conductive substance.

19. A circuitry module, comprising:

a plurality of dies, wherein at least one die includes a memory device;

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control, wherein the memory device includes a transistor in a periphery that is made from a method that includes:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to strap the dual-doped polycrystalline silicon line, the trench having a large cross-sectional area to decrease a horizontal resistance of the semiconductor device so as to increase the performance of the semiconductor device in the periphery.

20. A memory module, comprising:

a plurality of memory devices;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data, wherein at least one memory device of the plurality of memory devices includes a transistor in a periphery that is made from a method that includes:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to strap the dual-doped polycrystalline silicon line, the trench having a large cross-sectional area to decrease a horizontal resistance of the semiconductor device so as to increase the performance of the semiconductor device in the periphery.

21. An electronic system, comprising:

a plurality of circuit modules that includes a plurality of dies, wherein at least one die includes at least one memory device;

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control;

a user interface, wherein the at least one memory device includes a transistor in a periphery that is made from a method that includes:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to strap the dual-doped polycrystalline silicon line, the trench having a large cross-sectional area to decrease a horizontal

resistance of the semiconductor device so as to increase the performance of the semiconductor device in the periphery.

22. A memory system, comprising:

a plurality of memory modules that includes a plurality of memory devices;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller, wherein one of the memory device includes a transistor in a periphery that is made from a method that includes:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to strap the dual-doped polycrystalline silicon line, the trench having a large cross-sectional area to decrease a horizontal resistance of the semiconductor device so as to increase the performance of the semiconductor device in the periphery.

23. A computer system, comprising:

a processor;

a memory system that comprises a plurality of memory modules, one of the plurality of the memory modules comprises a plurality of memory devices;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller;

at least one user interface device, wherein the at least one user interface device includes a monitor;

at least one output device, wherein the at least one output device includes a printer;

at least one bulk storage device, wherein at least one memory device of the plurality of memory devices includes a transistor in a periphery that is made from a method that includes:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to strap the dual-doped polycrystalline silicon line, the trench having a large cross-sectional area to decrease a horizontal resistance of the semiconductor device so as to increase the performance of the semiconductor device in the periphery.

24. A method for strapping a gate structure in a periphery of a semiconductor device, the gate structure includes a polycrystalline silicon layer having a p-type strip abutting an n-type strip, the p-type strip and the n-type strip defining a length of the polycrystalline silicon layer, the method comprising:

exposing the polycrystalline silicon layer substantially along the length;

forming over the polycrystalline silicon layer a nonconductive stack that includes a stopping layer and a nonconductive layer, the stopping layer having a characteristic to stop an etching process once consumed by the etching process;

etching the nonconductive stack to expose the polycrystalline silicon layer substantially along the length to form a trench; and

filling the trench with a conductive stack having a silicide layer to reduce the vertical resistance of the gate structure and a conductive layer to reduce the horizontal resistance of the gate structure.

25. A method for making a semiconductor structure in a periphery, the method comprising:

forming a single polycrystalline line having a p-type strip adjoining an n-type strip;

forming a stopping layer over the single polycrystalline line, forming a nonconductive layer over the stopping layer;

forming a trench having a depth defined by etching the nonconductive layer until the act of etching stops when the stopping layer is etched away; and

filling the trench with a conductive stack that includes titantium, titanium nitride, and tungsten to reduce vertical resistance and horizontal resistance.

26. A method for strapping a semiconductor device in a periphery, comprising:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to strap the dual-doped polycrystalline silicon line, the trench having a large cross-sectional area to decrease a horizontal resistance of the semiconductor device so as to increase the performance of the semiconductor device in the periphery.

27. The method of claim 26, further comprising depositing on a substrate in the periphery the dual-doped polycrystalline silicon line.

28. The method of claim 27, wherein the dual-doped polycrystalline silicon line defines a gate line for the semiconductor device, and wherein the semiconductor device includes a surface p-channel transistor.

29. The method of claim 28, further comprising forming the nonconductive stack over the dual-doped polycrystalline silicon line in the periphery, the nonconductive stack includes the stopping layer and a borophosphorus silicate glass layer, the stopping layer subjacently abutting a borophosphorus silicate glass layer.

30. The method of claim 29, wherein the stopping layer includes a dielectric liner that is selected from a group consisting of tetrathylorthosilicate and dielectric-antireflective-coating compound.

31. The method of claim 30, wherein the stopping layer includes a thickness of about 300 angstroms.

32. A method for forming a routing in a periphery area of a semiconductor structure, comprising:

forming from a nonconductive stack a trench that superjacently abuts along a substantial length of a gate stack in the periphery, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the trench with a conductive stack to form the routing over the gate stack, the trench having a large cross-sectional area to decrease a horizontal resistance of the routing.

33. The method of claim 32, wherein the gate stack includes a gate oxide layer, a polycrystalline silicon layer formed on the gate oxide layer to act as a gate, a conductive layer formed on the polycrystalline layer to reduce resistance, and a gate cap layer formed on the conductive layer to electrically isolate the gate stack.

34. The method of claim 33, further comprising forming the nonconductive stack by depositing the stopping layer over the gate stack and a dielectric layer over the stopping layer.

35. The method of claim 34, wherein forming the trench includes photolithographing the nonconductive stack and etching the nonconductive stack until the act of etching is stopped when the stopping layer is consumed by the act of etching.

36. The method of claim 35, wherein etching includes dry etching the nonconductive stack.

37. The method of claim 36, wherein the conductive stack includes titanium.

38. A method for forming a contact to an active region in a periphery of a semiconductor structure, comprising:

forming from a nonconductive stack an opening that abuts an active region in the periphery, the nonconductive stack including a stopping layer that stops an etching process once etched away to define the bottom of the trench; and

filling the opening with a conductive stack to form a contact over the gate stack, the trench having a predetermined cross-sectional area to decrease a horizontal resistance of the contact.

39. The method of claim 38, wherein the active region is highly doped with donor impurities or acceptor impurities.

40. The method of claim 39, wherein the conductive stack includes a refractory metal and a silicide layer that decreases a vertical resistance of the contact.

41. The method of claim 40, wherein the conductive stack includes a barrier compound that is selected from a nitride compound.

42. The method of claim 41, wherein the conductive stack includes a conductive plug substance that is selected from tungsten.

43. The method of claim 42, wherein the act of forming the trench from the nonconductive stack includes a self-aligned contact (SAC) etching process.

44. A method for making semiconductor structures on a substrate having an array area and a periphery area, comprising:

forming from a nonconductive stack a number of openings to expose a number of semiconductor structures in the array area and in the periphery area, the nonconductive stack including a stopping layer to stop an etching process once etched away to define the bottom of each opening; and

filling the number of openings with a conductive stack having the characteristic to reduce a vertical resistance of each semiconductor structure and a horizontal resistance of each semiconductor structure so as to increase the performance of each semiconductor structure.

45. The method of claim 44, wherein forming a number of openings includes forming a first opening to expose a first active portion of the substrate and a first polycrystalline silicon gate of a first gate stack, the first active portion and the first gate stack proximately situated in the array area.

46. The method of claim 45, wherein forming a number of openings includes forming a second opening that longitudinally abuts along a substantial length of a dual-doped polycrystalline silicon line having a p-type strip adjoining an n-type strip, the dual-doped polycrystalline silicon line formed in the periphery area.

47. The method of claim 46, wherein forming a number of openings includes forming a third opening that superjacently abuts a gate cap layer of a second gate cap in the periphery area.

48. The method of claim 47, wherein forming a number of openings includes forming a fourth opening that superjacently abuts a second active portion of the substrate in the periphery area.

49. The method of claim 48, wherein filling the number of openings with a conductive stack includes filling at the bottom of each opening with a titanium layer, filling over the titanium layer with a layer of titanium nitride, and filling over the layer of titanium nitride with a tungsten layer.